Claims

[c1] What is claimed is:

1.A phase-locked loop comprising:

a phase detector for receiving an input signal and a feedback signal, and for outputting a phase error signal based on a phase difference between the input signal the feedback signal;

a signal reshaper connected to the phase detector for reshaping the phase error signal;

a charge pump connected to the signal reshaper for receiving the reshaped or unreshaped phase error signal from the signal reshaper and for outputting a charge pump signal;

a low pass filter connected to the charge pump for receiving the charge pump signal and outputting an output signal; and

a voltage-controlled oscillator connected between the low pass filter and the phase detector for receiving the output signal and for outputting a corresponding oscillation signal, wherein the feedback signal inputted into the phase detector is generated from the oscillation signal;

wherein the unreshaped phase error signal causes the charge pump to output a charge pump signal that changes the frequency of the feedback signal to match the frequency of the input signal, and the reshaped phase error signal causes the charge pump to output a charge pump signal that synchronizes the output signal with a target frequency.

[c2] 2.The phase-locked loop of claim 1 further comprising a frequency detector connected between the voltage-controlled oscillator and the charge pump for receiving the input signal and the feedback signal and for outputting a frequency difference signal to the charge pump.

[c3] 3.The phase-locked loop of claim 1 wherein when the frequency of the output signal is in a lower range that is lower than the target frequency, the signal reshaper reshapes the phase error signal to increase the frequency of the output signal out of the lower range; and when the frequency of the output signal is in an upper range that is above the target frequency, the signal reshaper reshapes the phase error signal to decrease the frequency of the

output signal out of the upper range.

[c4] 4.The phase-locked loop of claim 3 wherein the lower range and the upper range are frequency ranges where the unreshaped phase error signal is incapable of synchronizing the output signal with the target frequency.

[c5] 5.The phase-locked loop of claim 1 wherein the signal reshaper is a pulse reshaper and the phase error signal comprises up pulses and down pulses.

[c6] 6.The phase-locked loop of claim 5 wherein the pulse reshaper lengthens or shortens a period of a pulse of the phase error signal.

[c7] 7.The phase-locked loop of claim 5 wherein the pulse reshaper increases or decreases a width of a pulse.

[c8] 8.The phase-locked loop of claim 1 wherein the charge pump increases or decreases an amplitude of a current.

[c9] 9.The phase-locked loop of claim 1 further comprising a controller that controls the signal reshaper and the charge pump.

[c10] 10.The phase-locked loop of claim 1 wherein the input signal is an eight-to-fourteen modulation (EFM) signal and the output signal is a clock signal, and the phase-locked loop is incorporated into a controller of a compact disk (CD) drive or a digital versatile disk (DVD) drive.

[c11] 11.A phase-locked loop comprising:
a phase detector for receiving an input signal and a feedback signal, and for outputting a phase error signal based on a phase difference between the input signal the feedback signal;
a charge pump connected to the phase detector for receiving the phase error signal from the phase detector and for outputting a charge pump signal, the charge pump tunable by a control signal;
a low pass filter connected to the charge pump for receiving the charge pump signal and outputting an output signal; and
a voltage-controlled oscillator connected between the low pass filter and the phase detector for receiving the output signal and for outputting a

corresponding oscillation signal, wherein the feedback signal inputted into the phase detector is generated from the oscillation signal;
wherein according to the control signal, the charge pump is capable of outputting a charge pump signal that changes the frequency of the feedback signal to match the frequency of the input signal, and capable of outputting a charge pump signal that synchronizes the output signal with a target frequency.

[c12] 12.The phase-locked loop of claim 11 further comprising a frequency detector connected between the voltage-controlled oscillator and the charge pump for receiving the input signal and the feedback signal and for outputting a frequency difference signal to the charge pump.

[c13] 13.The phase-locked loop of claim 11 wherein when the frequency of the output signal is in a lower range that is lower than the target frequency, the charge pump reshapes the phase error signal to increase the frequency of the output signal out of the lower range; and when the frequency of the output signal is in an upper range that is above the target frequency, the charge pump reshapes the phase error signal to decrease the frequency of the output signal out of the upper range.

[c14] 14.The phase-locked loop of claim 13 wherein the lower range and the upper range are frequency ranges where the unreshaped phase error signal is incapable of synchronizing the output signal with the target frequency.

[c15] 15.The phase-locked loop of claim 11 wherein phase error signal comprises up pulses and down pulses and the charge pump as controlled by the control signal increases or decreases an amplitude of a current.

[c16] 16.The phase-locked loop of claim 11 wherein the input signal is an eight-to-fourteen modulation (EFM) signal and the output signal is a clock signal, and the phase-locked loop is incorporated into a controller of a compact disk (CD) drive or a digital versatile disk (DVD) drive.

[c17] 17.A method for synchronizing an output signal of a phase-locked loop with a target frequency comprising:
detecting a phase difference between a feedback signal and an input signal;

generating a phase error signal based on the detected phase difference between the feedback signal and the input signal;
reshaping the phase error signal by changing a period of a pulse of the phase error signal;
filtering the reshaped phase error signal to generate the output signal; and
generating an oscillation signal in proportion to the output signal, wherein the feedback signal inputted into the phase detector is generated from the oscillation signal.

[c18] 18.The method of claim 17 further comprising detecting a frequency difference between the feedback signal and the input signal.

[c19] 19.The method of claim 17 wherein reshaping the phase error signal comprises:
reshaping the phase error signal to increase the frequency of the output signal when the frequency of the output signal is in a lower range that is lower than the target frequency; and
reshaping the phase error signal to decrease the frequency of the output signal when the frequency of the output signal in an upper range that is above the target frequency;
wherein the lower range and the upper range are frequency ranges where the unreshaped phase error signal is incapable of synchronizing the output signal with the target frequency.

[c20] 20.The method of claim 17 wherein the phase error signal comprises up pulses and down pulses.